2W Ku-band Coplanar MMIC HPA using HBT for Flip-Chip Assembly

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ABSTRACT — **A coplanar HBT MMIC amplifier in Ku-band for space applications is presented. This HPA is based on the commercial HB20P process of UMS adapted to flip-chip assembly. An output power closed to 2W has been measured over 10.5-12.2GHz frequency range with an associated PAE higher than 25% and an associated gain of 20dB. The coplanar technology (CPW) and flip-chip mounting impact on the HPA design is also described.**

I. INTRODUCTION

Microstrip technology is classically used to design HPA at microwave frequencies. This allows to minimize the losses in the amplifier output matching networks in order to maximize the amplifier PAE. Another key point in HPA design for space applications is to guaranty a maximum junction temperature (typically below 115°C). The use of transistor with high power density such as HBT (3.5W/mm) implies to improve the thermal management. The flip-chip mounting is an attractive solution. Indeed, when the MMIC process is adapted, the flip-chip assembly allows to decrease drastically the thermal resistance. Unfortunately, the use of the flip-chip mounting techniques for microstrip HPAs can modified HPA performances. The alternative is to design the HPA in coplanar technology which confines the fields within the gaps on the CPW, minimizing the mounting substrate influence.

In APOS (Advanced High Frequency POwer Subassemblies) project [1] supported by European Commission, the thermal advantage of flip-chip mounting have been exploited. So HB20P process of United Microwave Semiconductors has been modified to add thermal bump near to HBT fingers. By this method, the HBT thermal resistance was dropped up to 30% in comparison with the standard process. In order to demonstrate the validity of the power flip-chip assembly, a MMIC HPA has been designed. For this design, CPW has been chosen to minimize flip-chip mounting effect on the HPA performances and to decrease the process cost.

In this paper, we present several steps of the HPA design. We emphasize on the performed simulations to choose the HPA are indicated. An output power higher than 2W at 11.7GHz has been measured with 28% associated power added and 20dB associated gain.

II.- MODEL

The HPA is based on the HB20P process of UMS [2] which was adapted to incorporate electroplated thermal and signal bumps at wafer level. In order to decrease the flip-chip assembly impact on the HPA performances, CPW has been chosen to design the HPA[3]. The coplanar library has been developed with the Coplan software for HP-EESOF's Libra serie IV simulator [4]. The non-linear HBT model has been obtained from I(V) and S-parameters pulsed measurements of HB20P standard HBT process [5]. It takes into account the thermal and non-quasi-static effects. The extrinsic elements of transistor model have been adjusted to take into account polymer used to reinforce air-bridge.

The coplanar library and non-linear HBT model have been validated thanks to measurements of several test patterns. For example, comparisons between measurements and simulations of a one stage amplifier (Figure 6) are presented Figures 7-9. They show the good accuracy of models.

III. DESIGN

The synthesis of the matching network of the amplifier last stage is very important for the power amplifier performances. This network has to present the optimum output load with the minimum losses. To minimize these ones, an electromagnetic simulation of coplanar lines has been performed with the COPLAN simulator. The cross section of the studied coplanar line is presented Figure 1. The losses variations versus line size are illustrated figure 2. The attenuation decreases when the ground to ground plane spacing (d) increases. Moreover for a fixed ground to ground plane spacing, the attenuation is minimum when the d/w ratio is about 2. However the best d/w ratio does not allow to decrease losses down to microstrip losses. This is an hard point to obtain low losses in the matching network of the last stage. Finally, in order to minimize these ones, we have chosen to work with ground to ground spacing at least equal to 150µm in the matching network.

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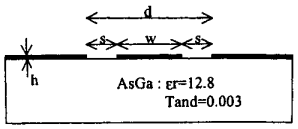

Figure 1- Cross section of coplanar transmission line

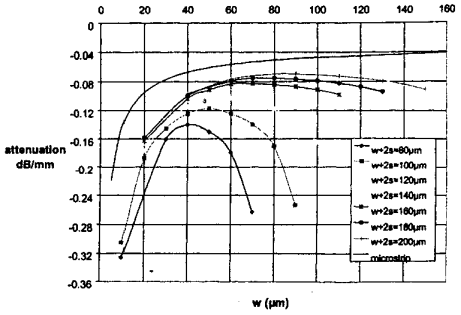

Figure 2 - Attenuation versus line widths for different ground to ground spacing values

Another point to take into account in the choice of the line dimensions is the influence of flip-chip mounting on the amplifier performance. So electromagnetic simulations with HFSS simulator have been performed to evaluate the transmission line impedance variations versus air gap, for several ground to ground spacing values (Figure 3 and Figure 4).

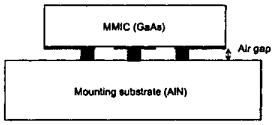

Figure 3 - A simplified view of MMIC Flip-chip reported

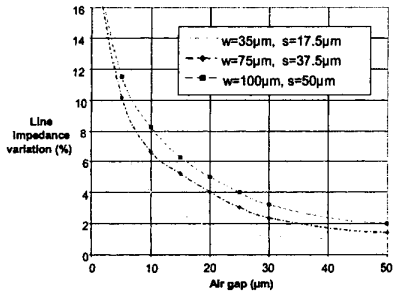

Figure 4 - Transmission line impedance versus air gap for several ground to ground spacing values

These curves show that the flip-chip report impact is more important when the ground to ground spacing increases. For an air gap of 25µm and a ground to ground spacing of 150µm, the percentage of change in the line impedance is about 3%. In order to evaluate the impact of these variations on the HPA performances, the ε_r of MMIC substrate of the last stage has been tuned from 12.8 to 13.7 in simulation (Figure 5).

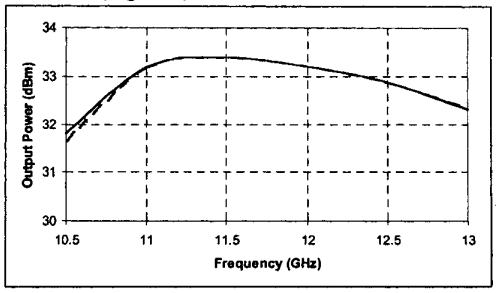

Figure 5 – HPA simulated Outpout power with two values of ε_r for the matching network of the last stage (12.8-13.7) (Pin=14.5dBm)

These simulations show that flip-chip mounting impact is very slight for an air gap of 25µm and a ground to ground spacing of 150µm. Hence, the matching network of the last stage has been designed with this ground to ground spacing. In this configuration, the losses matching network have been simulated about 1dB. They are higher than matching network losses in microstrip technology. So, the choice of CPW leads to a decrease of the amplifier PAE, but it is more compatible with the flip-chip mounting. On one hand, about 3 points of PAE have been lost, but on the other hand, the flip-chip mounting leads to decrease the thermal resistance of 30%. The second point is very interesting for space applications due to constraints on the junction temperature. Indeed, for most space applications, it needs to remain below 115°C. Hence, the decrease of the thermal resistance allows for the same transistor development to increase the bias and output power of the HPA up to 30% in comparison with standard transistor.

During APOS project, a Ku band HPA has been designed. It is composed of three stages. The last stage is composed of 4 transistors of 8 fingers 2*30µm. The HPA layout is presented Figure 10. Its size is 5.3x3mm². We can note the lines with a ground to ground spacing of 150µm in the last stage. Several methods have been used to make sure of the HPA stability in linear and non-linear operating conditions [6][7].

IV. MEASUREMENTS

The amplifier S-parameters have been measured on wafer under CW conditions at a fixed collector current density (figures 11-13). The amplifier gain is higher than 20dB over

the 10.5-12.2GHz frequency band with a low ripple. Input return losses and output return losses are respectively better than 18dB and 12dB over the frequency band. A low device to device dispersion can be observed on these figures. As the wafer was unthinned and the MMIC not flip-chip mounted the power measurements were performed in a pulse mode on the base in order to compensate the increase of the thermal resistance. These preliminary measurements show that the output power is closed to 33dBm over 10.5-12.2GHz frequency range with associated power added efficiency higher than 25% and associated gain about 20dB (figures 12 and 15).

V. CONCLUSIONS

A 2W MMIC HPA in Ku band developed for space applications has been presented. It has been designed with the HB20P process adapted for power flip-chip assembly. The decrease of the thermal resistance (up to 30%) obtained with this mounting technique is a very interesting point for space missions due to strong constraints on the junction temperatures for these applications. Many simulations have been also performed to minimize the CPW losses and to ensure low impact of flip-chip mounting on the HPA performances. For this coplanar amplifier, an output power higher than 2W at 11.7GHz has been measured with 28% associated power added and 20dB associated gain.

ACKNOWLEDGEMENT

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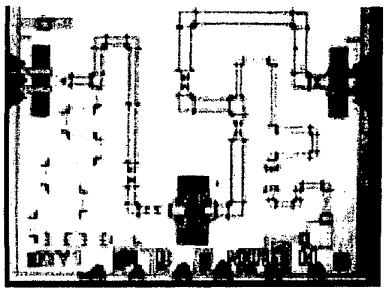


Figure 6- Picture of the one stage HPA

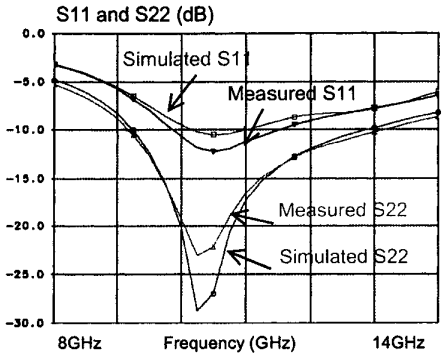


Figure 7 – Simulated and measured S11 and S22 parameters of the one stage HPA (Vce=5V, Jc=10kA/cm²)

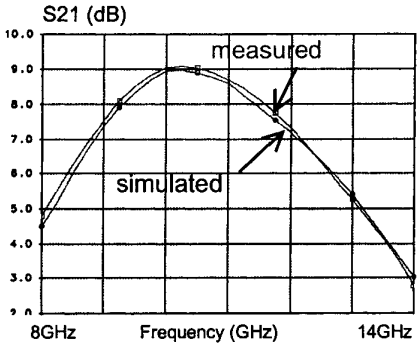
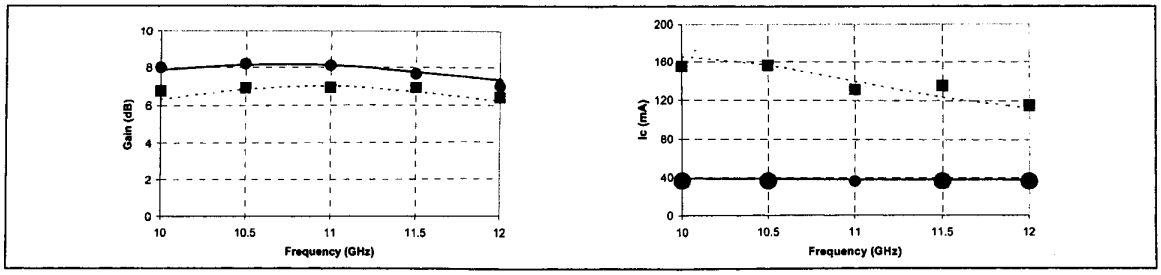


Figure 8 – Simulated and measured S21 parameters of the one stage HPA (Vce=5V, Jc=10kA/cm²)



___simulation (Pin=0dBm); ------ simulation (Pin=19dBm); ● ■ Measurements (Pin=0dBm; Pin=19dBm)

Figure 9 – Measured and simulated gain and collector current of one stage HPA versus frequency (Vce=8V)

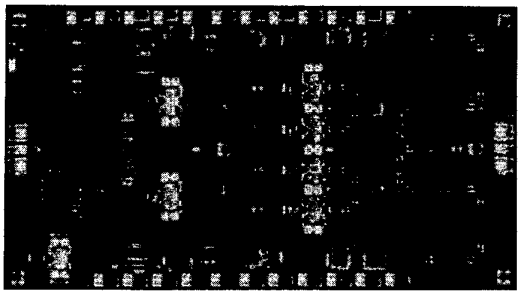


Figure 10 – HPA layout

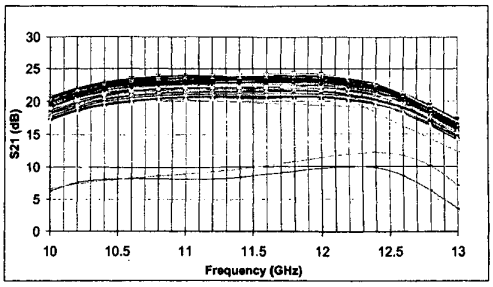


Figure 13 - Measured S21 of the HPA (Vce=5V,Jc=10kA/cm²)

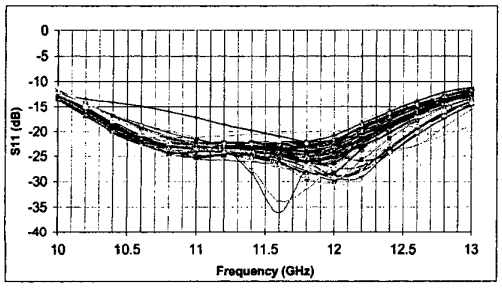


Figure 11 - Measured S11 of the HPA (Vce=5V,Jc=10kA/cm²)

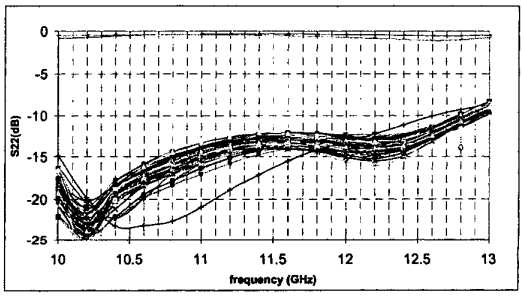


Figure 14 - Measured S22 of the HPA (Vce=5V,Jc=10kA/cm²)

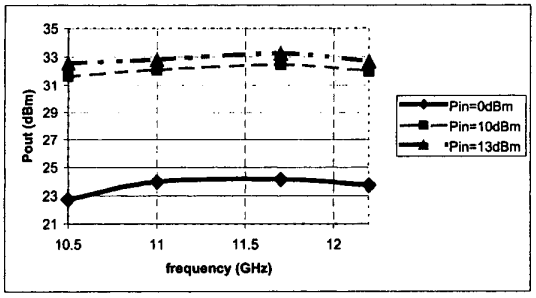


Figure 12 - Measured HPA output power versus frequency

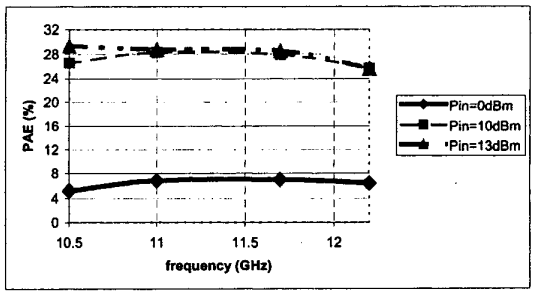


Figure 15 - Measured HPA PAE versus frequency